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<u>L34</u>	l16 and L29	19	<u>L34</u>
<u>L33</u>	l15 and L29	102	<u>L33</u>
<u>L32</u>	l14 and L29	239	<u>L32</u>
<u>L31</u>	l13 and L29	189	<u>L31</u>
<u>L30</u>	l12 and L29	377	<u>L30</u>
<u>L29</u>	branch\$3 near1 taken and l11	423	<u>L29</u>
<u>L28</u>	branch\$3 near3 taken and l11	483	<u>L28</u>
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<u>L26</u>	l11 and l16	21	<u>L26</u>
<u>L25</u>	l11 and l15	120	<u>L25</u>

<u>L24</u>	111 and 114	269	<u>L24</u>
<u>L23</u>	111 and 113	233	<u>L23</u>
<u>L22</u>	111 and 112	441	<u>L22</u>
<u>L21</u>	110 and 116	21	<u>L21</u>
<u>L20</u>	110 and 115	122	<u>L20</u>
<u>L19</u>	110 and 114	297	<u>L19</u>
<u>L18</u>	110 and 113	245	<u>L18</u>
<u>L17</u>	110 and 112	478	<u>L17</u>
<u>L16</u>	(718/101-108)[CCLS]	5154	<u>L16</u>
<u>L15</u>	(711/118-221)![CCLS]	27811	<u>L15</u>
<u>L14</u>	(712/230-248)[CCLS]	3464	<u>L14</u>
<u>L13</u>	(712/205-219,225-228)[CCLS]	6068	<u>L13</u>
<u>L12</u>	(712/2-300)[CCLS]	13638	<u>L12</u>
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<u>L11</u>	L10 and (buffer\$3 or fifo or lifo)	525	<u>L11</u>
<u>L10</u>	L9 and branch\$3	572	<u>L10</u>
<u>L9</u>	L7 and L8	591	<u>L9</u>
<u>L8</u>	(renear1 order\$3 or rearrang\$7 or out near2 (sequence or order))	5639954	<u>L8</u>
<u>L7</u>	L5 and (predict\$5 or speculat\$5) near15 (taken)	613	<u>L7</u>
<u>L6</u>	L5 and (predict\$5 or speculat\$5)	2056	<u>L6</u>
<u>L5</u>	(prefetch\$6 or fetch\$7) near10 (simultaneous\$4 or parallel\$5 or concurrent\$4)	6952	<u>L5</u>
<u>L4</u>	L3 not "non-volatile"	3	<u>L4</u>
<u>L3</u>	L1 and (map\$5 or associat\$4 or allocat\$5 or deallocat\$5) near8 (memor\$4 or space or region\$1 or section\$1 or range\$1 or area\$1 or location\$1 or block\$1 or segment\$1) NEAR55 VOLATILE	63	<u>L3</u>
<u>L2</u>	L1 and (map\$5 or associat\$4 or allocat\$5 or deallocat\$5) near8 (memor\$4 or space or region\$1 or section\$1 or range\$1 or area\$1 or location\$1 or block\$1 or segment\$1)	770	<u>L2</u>
<i>DB=PGPB,USPT; PLUR=YES; OP=OR</i>			
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» Key

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IEEE CNF	IEEE Conference Proceeding
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IEEE STD	IEEE Standard

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- ☐ 4. **Microarchitectural support for precomputation microthreads**
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- ☐ 7. **The Speculative Prefetcher and Evaluator Processor for Pipelined Memory Hierarchies**
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- ☐ 8. **Slipstream execution mode for CMP-based multiprocessors**
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- ☐ 9. **TCP: tag correlating prefetchers**
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- ☐ **18. A distributed colouring algorithm for control hazards in asynchronous pipelines**
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